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Notice of Allowability	Application No.	Applicant(s)	
	10/670,829	FAN ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on February 9, 2007 and interview summary.*.

2. ☒ The allowed claim(s) is/are *1-5,8-15,18 and 19*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Harden E. Stevens, III (Reg. 55,649) on April 25, 2007.

The application has been amended as follows: Amend the claims as below:

Claim 1: (Currently amended) A circuit board comprising:

first and second reference plane layers where the inner surface of each layer is separated by and in contact with a dielectric layer;

an embedded discrete surface mount first decoupling capacitor mounted to the outer surface of the first reference plane layer, the first decoupling capacitor comprising a first electrode connected to the first reference plane and a second electrode ~~connected to the second reference plane~~;

a first buried via electrically contacted to the second electrode of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer;

an embedded discrete surface mount second decoupling capacitor mounted to the outer surface of the second reference plane

layer, the second decoupling capacitor comprising a first electrode connected to the second reference plane and a second electrode ~~connected to the first reference plane; and~~ ;

a second buried via electrically contacted to the second electrode of the second decoupling capacitors, the second buried via extending through the second reference plane layer and the dielectric layer to electrically contact the first reference plane layer; and

vias extending generally along a direction perpendicular to the first and second reference plane layers,

wherein the first and second decoupling capacitors are aligned generally along the direction and overlapping one another to increase an amount of space in the circuit board through which the vias are extendable.

Claim 6-7: cancel.

Claim 8: Delete "7" and add - - 5 - -, line 1.

Claim 13: (previously amended) A system comprising:

a power supply;

an integrated circuit device to be powered by the power supply; and

a circuit board on which the integrated circuit device is mounted, the circuit board comprising:

first and second reference plane layers where the inner surface of each layer is separated by and attached to a dielectric layer;

embedded discrete surface mount first decoupling capacitors mounted to the outer surface of the first reference plane layer, the first decoupling capacitors being spaced apart across the outer surface of the first reference plane layer and each of the first decoupling capacitors includes a first electrode connected to the first reference plane layer and a second electrode;

a first buried via electrically contacted to the second electrode of one of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer;

embedded discrete surface mount second decoupling capacitors mounted to the outer surface of the second reference plane layer,

the second decoupling capacitors being spaced apart across the outer surface of the second reference plane layer and each of the second decoupling capacitors includes a first electrode connected to the second reference plane and a second electrode;

a second buried via electrically contacted to the second electrode of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer;

vias extending generally perpendicular to the first and second reference plane layers; and

wherein each pair of the first and second decoupling capacitors are aligned in an overlapping manner generally along a direction

that is perpendicular to the first and second reference plane layers to increase an amount of space in the circuit board for the vias.

Claim 16-17: cancel.

Claim 18: Delete "17" and add - - 15 - -, line 1.

Claims 20-26: cancel.

2. Claims 11 and 12, previously withdrawn form consideration as a result of restriction requirement are hereby rejoined as they include all the limitation of the allowable base claim 3.

3. The following is an examiner's statement of reasons for allowance:

Regarding claims 1-5 and 8-12:

A circuit board structure with embedded decoupling capacitor with the limitations "a first buried via electrically contacted to the second electrode of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer;" and "a second buried via electrically contacted to the second electrode of the second decoupling capacitors, the second buried via extending through the second reference plane layer and the dielectric layer to electrically contact the first reference plane layer;" in combination with the other claimed limitations of the base claim 1 has not been fairly taught or suggested by the prior art of record.

Regarding claims 13-15 and 18-19:

A circuit board structure with embedded decoupling capacitors with the limitations "a first buried via electrically contacted to the second electrode of one of the first decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer;" and "a second buried via electrically contacted to the second electrode of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer;" in combination with the other claimed limitations of the base claim 13 has not been fairly taught or suggested by the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IBPatel

ibp
April 26, 2007

Ishwar (I. B.) Patel
Primary Examiner